Indian Institute of Technology Kanpur

INSTITUTE LECTURE SERIES

February 15 (Wednesday) | 4.00 pm | L - 15

Speaker: Prof. Subramanian S. Iyer

Talk Title: Advanced Packaging - Chiplets, Dielets and Heterogeneous Integration

About the Speaker

Subramanian S. Iyer (Subu) is Distinguished Professor and holds the Charles P. Reames Endowed Chair in the Electrical Engineering Department and a joint appointment in the Materials Science and Engineering Department at the University of California at Los Angeles. He is the Director of the Center for Heterogeneous Integration and Performance Scaling (UCLA CHIPS). Prior to that he was an IBM Fellow. His key technical contributions have been the development of the world's first SiGe base HBT, Salicide, electrical fuses, embedded DRAM and 45nm technology node used to make the first generation of truly low power portable devices as well as the first commercial interposer and 3D integrated products.

He has been exploring new packaging paradigms and device innovations that may enable wafer-scale architectures, in-memory analog compute and medical engineering applications. He is a fellow of IEEE, APS, iMAPS and NAI as well as a Distinguished Lecturer of IEEE EDS and EPS. He is on the Board of Governors of IEEE EPS. Prof. Iyer is a Distinguished Alumnus of IIT Bombay and received the IEEE Daniel Noble Medal for emerging technologies in 2012 and the 2020 iMAPS Daniel C. Hughes Jr Memorial award and the iMAPS distinguished educator award in 2021. Prof. Iyer is currently Prof. Ramakrishna Rao Visiting Chair Professor at CeNSE, IISc, Bengaluru.

Abstract of the Talk

Packaging is undergoing a major paradigm shift and promises to take up the lag caused by the slowing down of CMOS scaling. In this talk, the speaker will examine these shifts that have been driven by the scaling of key packaging metrics such as bump pitch, trace pitch, inter-die spacing and alignment. The goal of advanced packaging is to enable the same benefits that Moore/Dennard scaling has accomplished for CMOS viz. density, performance, power, and cost and can make packaged chip assemblies comparable to monolithic SoCs using these metrics with the additional advantage of heterogeneity. The vehicles that advanced packaging employs are somewhat different: dielets/chiplets, advanced assembly techniques, simplified inter-chip communication protocols and cost optimization via the use of optimized heterogeneous technologies. Another important aspect of advanced packaging is the adoption and adaptation of silicon technology methods to packaging. He will discuss the technologies and some instantiation examples that they have developed at UCLA.

All are cordially invited to attend

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