[Scdt] SCDT-FlexE Centre Weekly Tuesday Seminar - 24.05.2022 at 7:30 PM

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Date 2022-05-23 16:24
Priority Normal

Zoom Meeting for joining the webinar:
https://zoom.us/j/99863678964?pwd=ZVJvdFN5T1UyQjdZbmxwS0htRUJOUT09

Meeting ID: 998 6367 8964
Passcode: 064022
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Dear Colleagues,

All integrated circuits (chips) built will need some form of packaging when used in the real world. In the coming years, packaging will be a critical component of Indian electronics manufacturing. This week, as part of the SCDT-FlexE Centre Weekly Tuesday Seminar, we have Prof. Nilesh Badwe of MSE Dept. who is an expert in this area and is passionate about this important field, will be sharing some technical challenges that he and his team overcame at Intel (where Nilesh used to work earlier). The low-temperature solder he will be discussing has important implications for flexible electronics which has restrictions on the temperatures of processing. Please join us on Zoom on Tuesday, 24th May at 7:30 PM.

With regards
S.K.I.

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Weekly Seminar Title:
“SnBi based Low-Temperature Solders for Packaging Applications”

Date: 24th May, 2022
Time: 7:30 PM to 8:30 PM
Zoom link details for the event is given above

Abstract of talk:
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There has been a significant interest in low-temperature solder (LTS) alloys for interconnect applications in the last 5-6 years. The low melting SnBi based materials help reduce the reflow temperatures during surface mount technology from 240C to below 190C. This reduction ensures significantly lower package warpage, enabling aggressive form factor and fine pitch packages while reducing the power consumption and overall carbon footprint of the manufacturing process. The legacy SnBi-based alloys, however, possessed their own challenges, including poor ductility and low reliability. The talk will discuss how different process and material based approaches were used to overcome the LTS specific new defect modes and improve the reliability, enabling their use in high volume manufacturing.

Bio:
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Nilesh Badwe is currently an Assistant Professor in the Department of Materials Science and Engineering at IIT Kanpur. Prior to this, he worked as a Packaging R&D Engineer, Staff Packaging R&D Engineer, and Materials Technologist in the Assembly Test Technology Division at Intel Corporation, USA for over 5.5 years. Nilesh obtained his B.Tech. in Metallurgical Engineering and Materials Science from IIT Bombay and his Ph.D. in Materials Science and Engineering from Arizona State University. He is an Associate Editor for the journal "Microelectronics Reliability". He also serves on the technical committees of Electronics Packaging and Interconnect Material - TMS, and the Surface Mount Technology Association.

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